ORIGINALLY SUBMITTED INFORMAL DRAWINGS

Serial No. 08/999,663

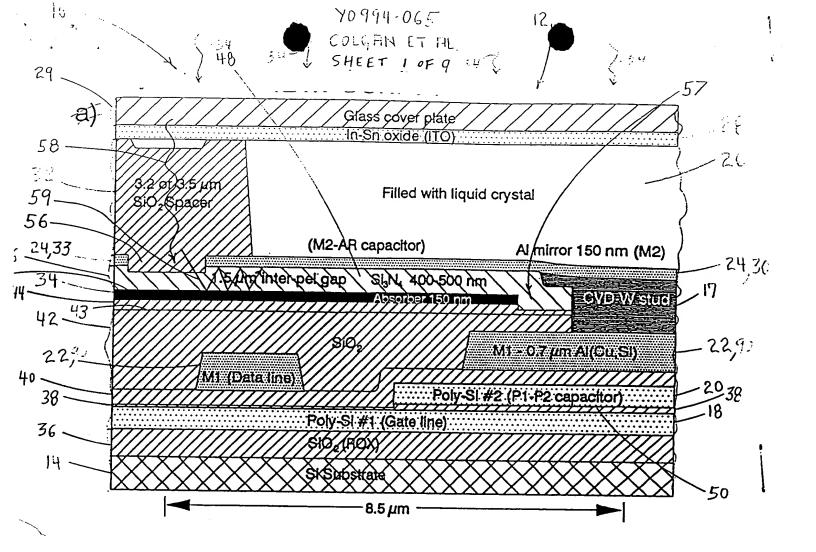
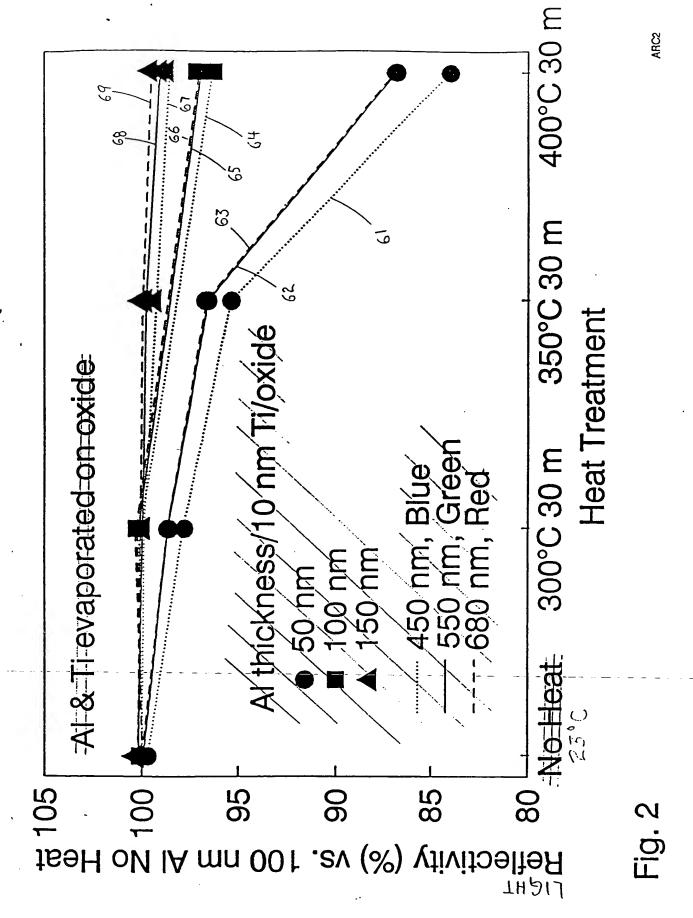
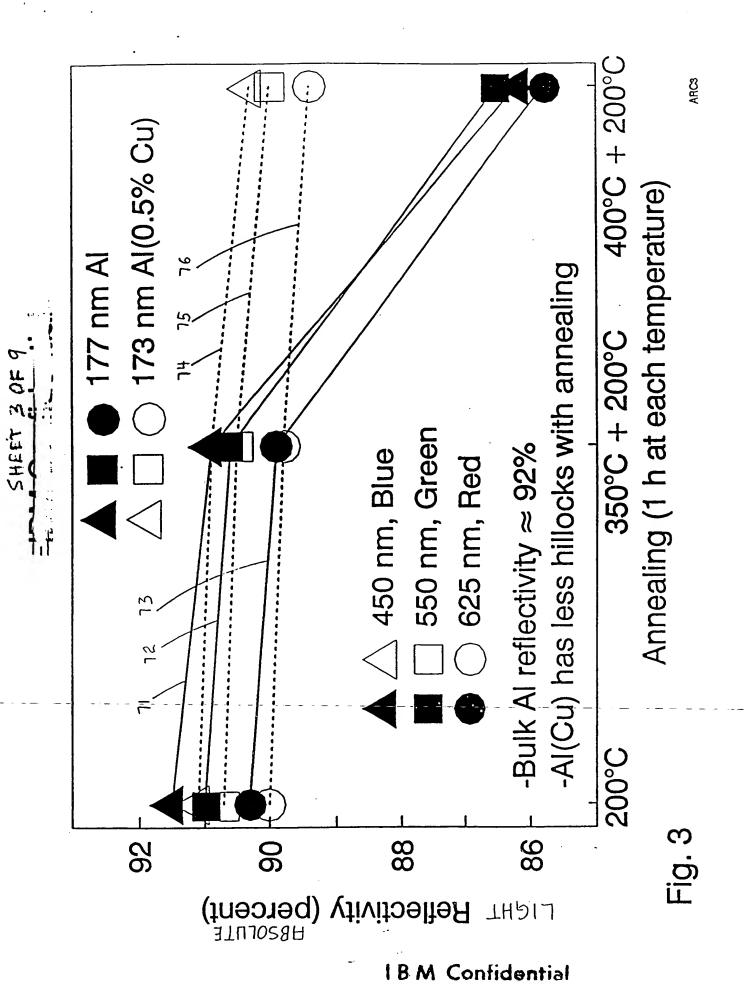


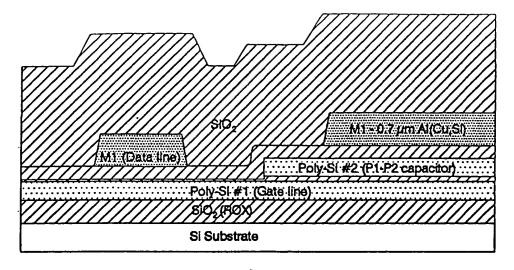
FIG 1





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a) Liftoff 0.7 μ m AI(Cu,Si) M1. Deposit thick oxide.

FIG 5

M1 (Data:line) M1 (Data:line) Poly-Si #2 (P1-P2 capacitor)
Poly-Si #1 (Gate line)
//////////////////////////////////////
Si Substrate

b) CMP oxide leaving 500 nm on highest M1 point.Deposit 200 nm oxide.

F16 6

	Si3V, x00-500,nm
	Absorber 150 pm
	//////////////////////////////////////
	/SiO ₃ ////////////////////////////////////
M1 (Data line)	///////////////////////////////////////
	Poly-Si.#2 (P1-P2 capacitor)
Pol	y-Si #1 (Gate line)
	\$\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
Sis	Substrate

c) Deposit 10 nm Tt/ 100 nm Al/ 50 nm TiN, pattern with AR mask.
Deposit 400-500 nm nitride.

FIG 7

Fig. 5(a-c)

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Si, N. 400-500 hm

Absolute Iso nin

M1 - 0.7 µm Al(Cu;Si)

M1 - 0.7 µm Al(Cu;Si)

Poly-Si #2 (P1-P2 capacitor)

Poly-Si #1 (Gate line)

Si Substrate

d) Pattern with V1 mask.
 Deposit liner & CVD-W.
 W Chem-mech polish.

FIG 8

	Al mirror 150 nm (M2)
1,5 Jun ligter-pel, gap St	N. 400-500 nhp DS013191 150 nm
	M1 = 0.7 μm·Al(Cu,Sl)
Mi. (Cata line)	Poly-Si #2 (P1-P2 capacitor)
Poly-SI #11	(Gate-line)
Si Substrate	3 .

e) Deposit 10 nm Tl/ 150 nm Al, pattern with M2 mask.

(M2-AR capacitor)

Al mirror 150 nm (M2)

1.5 m Intel pel gala Sign, 400-500 nm

(Data time)

Poly-Si #2 (P1-P2 capecifor)

Poly-Si #1 (Gate line)

Si Substrate

 Deposit 2.2 or 3 μm oxide, pattern with SP mask. Open up M1 pads with TV mask.

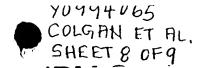
Fig. 5(d=f) Fig 10

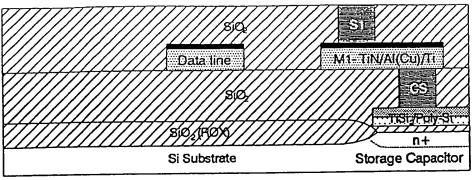
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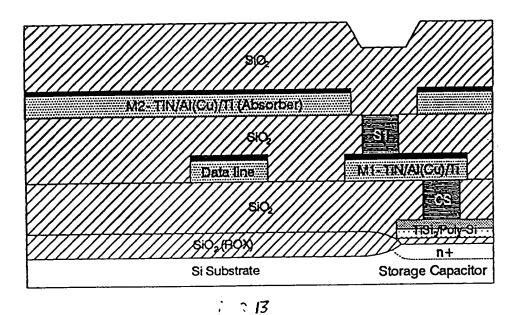
a) 15 μm



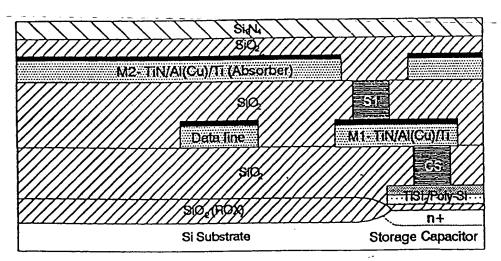


a) Use standard CMOS 4 process to S1.

F 6 12



 b) Pattern POR M2 as Absorber layer. POR oxide deposition.



on highest M2 point.

Deposit 300 nm nitride.

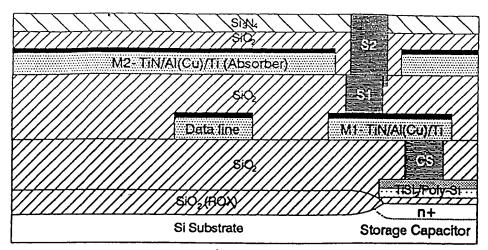
Fig. 8(a-c)

15 14

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d) Pattern with S2 mask. Deposit liner & CVD-W. W Chem-mech polish. Stacked S1&S2 to connect M1 & M3.

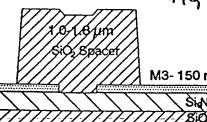
FIG 15

M3-150 nm Al or Al(Cu)/10 nm Ti (Mirror)

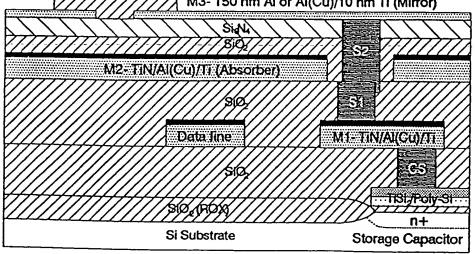
M2-TIN/Al(Cu)/TI (Absorber) Data line MISTIN/A(Cu)/TI e) Deposit 10 nm Ti/ 150 nm Al, pattern with M3 mask.

F19 16

Si Substrate



M3-150 nm Al or Al(Cu)/10 nm Ti (Mirror)



f) Deposit 1.0 or 1.8 μ m oxide, pattern with SP mask. Open up M2 pads with TV mask.

F19:17

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Storage Capacitor